EC-307	HDL PROGRAMING	L	T	P	C
		4	-	-	3

COURSE OBJECTIVES:

1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design.
2. To know the behavioural modeling of combinational and simple sequential circuits.
3. To know the behavioral modeling of algorithmic state machines.
4. To know the synthesis of combinational and sequential descriptions.
5. To know the architectural features of programmable logic devices.

COURSE OUTCOMES:

After successful completion of the course, the students are able to

1. demonstrate HDL design flow, Digital circuits design, Switch De-bouncing, Metastability and Programmable logic devices.
2. design combinational and sequential circuits using HDL Programming Language.
3. solve algorithmic state machines using Hardware description language.
4. analyze process of synthesizing the combinational and sequential descriptions.
5. memorize advantages of programmable logic devices and their description in Verilog.

UNIT I *Text Book - 1,2* **(12)**

Introduction to Logic Design with Verilog : Structural models of combination logic, logic simulation, design verification, test methodology, propagation delay, truth table models of combinational and sequential logic with verilog modules, ports, gate types, gate delays, dataflow modelling, continuous assignments delays, expressions, operators, operands, operator types

UNIT II *Text Book - 1* **(12)**

Logic Design With Behavioral Models of Combinational And Sequential Logic : Behavioral modeling, data types for behavioral modeling, behavioral models of combinational logic, propagation delay and continuous assignments, lathes and level sensitive circuits in verilog, cyclic behavioural models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modeling.

UNIT III *Text Book - 1* **(10)**

Behavioral models of multiplexers, encoders and decoders data flow model of a lfsr machines with multicycle operations, algorthmic state machine charts for behavioral modeling, asmd charts, behavioral models of counters, shift registers and register files, switch debounce, metastability, synchronizers for asynchronous signals.

UNIT IV *Text Book - 1* **(10)**

Introduction to synthesis : synthesis of combinational logic, synthesis of sequential logic with latches, synthesis of three state devices and bus interfaces, synthesis of sequential logic with flip flops, synthesis of explicit state machines registered logic.

UNIT V *Text Book - 1* **(10)**

Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.

LEARNING RESOURCES:

TEXT BOOK(s):

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009.

2. Samir Palnitkar - Verilog HDL, 2nd edition, Pearson Education, 2003.

REFERENCE BOOK(s):

1. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.
2. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.

WEB RESOURCES:

1. http://nptel.ac.in/video.php?subjectId=106105083
2. http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-884-complex-digital-systems-spring-2005/lecture-notes/