EC-252   **DIGITAL LOGIC DESIGN LAB**   **L T P C**
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COURSE OBJECTIVES:

1. To design Combinational logic circuits such as adders and subtractors.
2. To design comparators, decoders multiplexers and demultiplexers.
3. To design Sequential logic circuits such as flip-flops and shift registers.
4. To design synchronous and asynchronous counters.

COURSE OUTCOMES:
After successful completion of the course, the students are able to
1. design and verify the functionality of logic gates
2. design and verify the functionality of combinational circuits.
3. design and verify the functionality of sequential circuits.
4. design and verify the functionality of synchronous and asynchronous sequential circuits.

List of Experiments:

1. Verification of logic gates using ICs.

2. Realization of Gates using Universal Building Block (NAND only).

3. Design of Combinational Logic Circuits like Half-adder, Full-adder, Half-Sub tractor and Full-Sub tractor.

4. Verification of 4-bit Magnitude Comparator.

5. Design of Decoders (BCD - Decimal decoder).

6. Applications of IC Parallel Adder (1's & 2's compliment addition).

7. Design of Code Converters (Binary to Gray).

8. Design of Multiplexers/De Multiplexers.

9. Verification of excitation Table of Flip-Flops using Gates.

10. Design of Shift register (To Verify Serial to parallel, parallel to Serial, Serial to Serial and parallel to parallel Converters) using Flip-Flops.

11. Design of Ring & Johnson Counters using Flip-Flops.

12. Conversion of Flip-Flops (JK-T, JK - D).

13. Design of Binary/Decade Counter.

14. Design of Asynchronous Counter, Mod Counter, Up Counter, Down Counter & Up/Down Counter.

15. Design of Synchronous Counter, Mod Counter, Up Counter, Down Counter & Up/Down Counter.

Note: A minimum of 10(Ten) experiments have to be performed and recorded by the candidate to attain eligibility for Semester End Practical Examination.