EC/EE-203	DIGITAL LOGIC DESIGN	L	T	P	C
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COURSE OBJECTIVES:

Students will be able to know

1. theorems and functions of Boolean algebra and behaviour of logic gates.
2. Boolean functions simplification using Karnaugh maps and Quine-McCluskey methods
3. combinational circuits design procedure and implementing them using PLDs
4. the behaviour and design of simple sequential circuits
5. the operation and design methodology for synchronous sequential circuits and Algorithmic State Machines

COURSE OUTCOMES:

After successful completion of the course, the students are able to

1. demonstrate the knowledge in properties and postulates of Boolean algebra, Minimization of switching functions using Map method and Tabular method, Combinational and sequential logic circuits, Programmable Logic Devices and ASM charts.
2. analyze combinational and sequential logic circuits.
3. design combinational and sequential circuits.
4. implement combinational logic circuits using PLDs.
5. design Synchronous Sequential Circuits using ASM charts.

UNIT I **(13)**

Signed Numbers and Complements, Addition and Subtraction Using R's and (r-1)'s Complements, Codes.Boolean Algebra and Combinational Networks: Definition of A Boolean Algebra, Boolean Algebra Theorems, Boolean Theorems and Functions, Canonical Formulas, Manipulation of Boolean Formulas, Gates and Combinational Networks, Incomplete Boolean Functions and Don't Care Conditions, Additional Boolean Operations and Logic Gates.

UNIT II **(13)**

Karnagh Maps (upto five variables): Using Karnaugh Maps to Obtain Minimal Expressions for Complete Boolean Functions, Minimal Expressions of Incomplete Boolean Functions.

Quine-McCluskey Method: The Quine-McCluskey Method of Generating Prime Implicants and Prime Implicates, Prime Implicants / Prime Implicates Tables and Irredundant Expressions, Prime Implicants / Prime Implicates Table Reductions, Decimal Method for Obtaining Prime Implicants.

UNIT III **(13)**

Combinational Circuits: Binary Adders, Subtractors, Decimal Adders, Comparators, Decoders, Encoders, Multiplexers. PLDs, PROMs, PLAs, PALs.

UNIT IV **(13)**

Sequential Elements : Latches, Timing Considerations, Master-Slave Flip-Flops, Edge Triggered Flip-Flops, Characteristic Equations.

Sequential Circuits : Registers, Counters, Design of Synchronous Counters.

UNIT V **(13)**

Synchronous Sequential Networks: Structure and Operation of Clocked Synchronous Sequential Networks, Aynalysis of Synchronous Sequential Networks, Modeling Clocked Synchronous Sequential Network Behaviour.

Algorithmic State Machines: The Algorithmic State Machine, ASM Charts, Examples of Synchronous

Sequential Network, Design using ASM Charts, State Assignments, ASM tables.

LEARNING RESOURCES:

TEXT BOOK(s):

Donald D. Givone - Digital Principles and Design, TMH, 2003.

REFERENCE BOOK(s):

1. Thomas L. Floyd - Digital Fundamentals, 10th Edition, Person Education, 2011
2. Brown-Vranesic - Fundamentals of Digital Logic with with Verilog Design, 3rd edition, TMH, 2013.

WEB RESOURCES:

http://nptel.iitm.ac.in/courses/